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A Note on Experimental Determination of Small-Signal Equivalent Circuit of Millimeter-Wave FETs

A. Eskandarian and S. Weinreb

***Abstract*—New expressions for determination of the parasitic inductances L_g, L_d, and L_s in the small-signal equivalent circuit of high-frequency Field Effect Transistors (FET's) are derived, based on the "active/passive" (also known as "hot/cold") measurement technique developed in literature. These equations are required when the size of parasitic capacitances is such that their effect on the forward-biased gate measurement cannot be ignored, as has been the case with our millimeter-wave transistors. The method produces an equivalent circuit which has been used successfully for design of multi-stage amplifiers at 60 and 94 GHz.**

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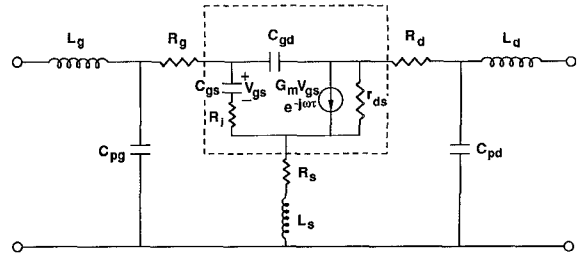

Fig. 1. The small-signal equivalent circuit of the FET's including the parasitic elements. The intrinsic FET model is shown in the dashed box.

I. INTRODUCTION

The most common method for determination of the equivalent circuit of a microwave Field Effect Transistor (FET) has been through minimization of the difference between measured and computed S-parameters versus frequency. However this procedure may not produce unique element values for the equivalent circuit and the dependence of element accuracy upon measurement accuracy is unclear. Dambrine *et al.* [1] and Berroth and Bosch [2], [3] recently presented methods that include S-parameters of the FET biased into a "passive" state, such as pinch-off or forward-biased gate, to provide additional data on the equivalent circuit. With this additional data it is possible to uniquely determine equivalent circuit values from measurements at a *single frequency*. Multiple-frequency measurements can then be utilized to test the accuracy of the data and the correct topology of the equivalent circuit as manifested by invariance of the element values with frequency.

The purpose of this letter is to make a necessary addition to the equations given in [1]–[2] and present experimental data showing invariance of equivalent circuit values from 1 to 18 GHz.

II. BACKGROUND

In "active/passive" measurement techniques, the equivalent circuit is conceptually divided into intrinsic and extrinsic parts. In a commonly used FET equivalent circuit shown in Fig. 1, the intrinsic part is shown in a dashed box. The extrinsic part includes the parasitic elements, i.e., the source, drain and gate resistances, and any additional inductances or capacitances which may exist due to the device layout, via holes, bonding pads, etc.

The parasitic elements are determined from the "passive" FET measurements, where the FET is biased similar to a diode, i.e., with zero voltage on the drain terminal. In this mode of operation the intrinsic part of the FET model in Fig. 1 should be replaced with an appropriate diode model that will depend on the bias voltage on the gate. Two types of gate biasing can be employed.

In the first type, a gate bias is chosen such that the channel under the gate is completely pinched off. This usually means a negative gate voltage. The drain and source terminals are at zero potential. The capacitive components of the equivalent circuit are dominant under this bias condition. The circuit diagram for this case is shown in Fig. 2, where it is assumed that the gate-source and gate-drain capacitances are equal to C_b (actually, depending on the lay-out structure of a FET, there is a small difference between these two capacitances). The measured S-parameters show capacitive behavior and are converted to Y-parameters. The value of C_b is determined from the imaginary part of Y_{12}. The values of C_{pd} and C_{pg} can then be determined from the imaginary parts of Y_{22} and Y_{11} simply by removing the contribution of C_b to these Y-parameters.

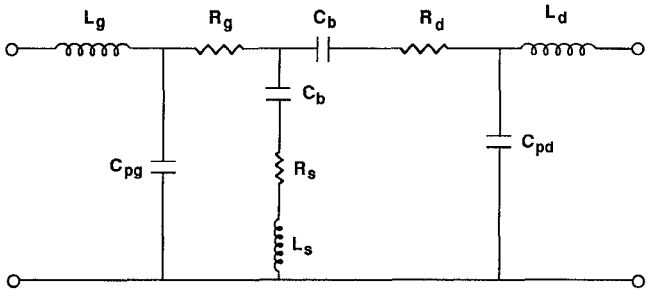

Fig. 2. The FET equivalent circuit under pinch-off condition with zero drain voltage.

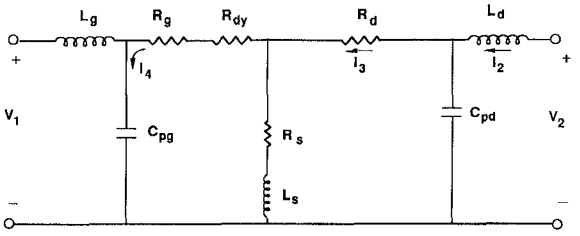

Fig. 3. The FET equivalent circuit under forward-biased gate voltage and zero drain voltage. The contribution of the channel resistance under the gate is ignored.

For the second type, the gate is forward biased with source and drain at zero potential. The gate currents are sufficiently large so that the internal device capacitances are all shunted with small resistors. The circuit model for this bias is shown in Fig. 3. The measured S-parameters are expected to show inductive behavior and are converted to Z-parameters. The values of resistors R_s, R_d, and R_g are determined from the real part of the Z-parameters, and the inductor values L_g, L_d, and L_s from the imaginary parts. More specifically, the value of L_s is directly determined from the imaginary part of Z_{12}. L_d and L_g can then be determined from the imaginary parts of Z_{11} and Z_{22}.

For the "active" measurements, the FET is biased to a point intended for circuit operation (with positive drain voltage, in the flat region of drain-source I-V characteristics). To remove the effect of parasitics in series branches, the measured S-parameters are converted to Z-parameters and the contribution of parasitics is subtracted. For parasitic elements in parallel branches, a conversion to Y-parameters is made. Continuing this procedure three times, one determines the Y-parameters of the intrinsic FET, from which the values of the small-signal circuit elements can be determined [2].

When the prior "passive" FET measurements were applied to our millimeter-wave devices, some of the S-parameters showed capacitive behavior under forward-biased gate operation, contrary to the expectations based on the arguments presented for the second case above. Specifically, the imaginary part of Z_{12} was negative. Because we believed that the parasitic capacitive elements were dominating the forward-biased measurements, we had to derive new expressions for the Z-parameters which included the effect of parasitic capacitances. In the following section we present the equations used for "passive" FET measurements and the results for a pseudomorphic Modulation Doped FET (MODFET).

III. Experimental Procedure and Results

The first step in the measurement procedure was to determine the parasitic capacitances C_{pd} and C_{pg}. The drain voltage was zero, and the gate was biased such that the FET channel was completely pinched off. The measured two-port S-parameters were converted to Y-parameters. Then, using the equivalent circuit of Fig. 2, we determined the values of C_{pd}, C_{pg}, and C_b from the following equations.

$$\mathrm{Im}(Y_{11}) = \omega(C_{pg} + 2C_b) \tag{1a}$$

$$\mathrm{Im}(Y_{12}) = -\omega C_b \tag{1b}$$

$$\mathrm{Im}(Y_{22}) = \omega(C_{pd} + C_b) \tag{1c}$$

Next, the gate was forward biased with zero drain voltage with the equivalent circuit as shown in Fig. 3, and the S-parameters were measured and consequently converted to Z-parameters.

The resistance of the channel under the gate (R_{ch}) is not included in the circuit of Fig. 3. This is justified for our devices since the gate length is about 0.1 μm which is small compared to the gate-source and gate-drain separations of about 0.9 μm. In addition, analysis of forward-biased gate operation [4] has shown that only a fraction of R_{ch} appears in series with parasitic resistances R_g, R_s, and R_d. These considerations validate the above approximation.

The circuit of Fig. 3 can be used to determine the Z-parameters under forward biased gate operation. Considering Z_{12} we can write

$$Z_{12} = \frac{V_1}{I_2} = \frac{I_4\left(\dfrac{1}{j\omega C_{pg}}\right)}{I_2} \tag{2}$$

where terminal 1 is in the open circuit condition. Using current divider relations we have

$$\frac{I_4}{I_3} = \frac{R_s + j\omega L_s}{R_g + R_{dy} + R_s + j\omega L_s + \dfrac{1}{(j\omega C_{pg})}} \tag{3}$$

and

$$\frac{I_3}{I_2} = \frac{\dfrac{1}{j\omega C_{pd}}}{R_s + j\omega L_s + R_d + \dfrac{1}{j\omega C_{pd}}} \tag{4}$$

where all the currents are defined in Fig. 3, R_{dy} is the dynamic resistance of the diode given by $R_{dy} = nkT/qI_g$, n is the ideality factor, k is Boltzman's constant, T is temperature, and I_g is the dc diode current. It should be noted that for the first term in the denominator of (4) we have assumed that the branch including (R_s and L_s) has a much lower impedance than that including (R_g and C_{pg}). This assumption is valid for the frequencies of interest. Combining (2), (3), and (4) and ignoring the terms of order (ω^2), which are small, we can derive an expression for Z_{12}. A similar type of analysis can be performed for Z_{22} and Z_{11}. Hence, the following expressions can be written for the real and imaginary parts of the $Z-$parameters

$$\mathrm{Real}(Z_{11}) = R_g + R_s + R_{dy} \tag{5a}$$

$$\mathrm{Real}(Z_{12}) = R_s \tag{5b}$$

$$\mathrm{Real}(Z_{22}) = R_s + R_d \tag{5c}$$

$$L_s = \frac{\mathrm{Im}(Z_{12})}{\omega} + \left[(R_s + R_{dy} + R_g)C_{pg} + (R_s + R_d)C_{pd}\right](R_s) \tag{6a}$$

$$L_d = \frac{\mathrm{Im}(Z_{22})}{\omega} - L_s + C_{pd}(R_s + R_d)^2 \tag{6b}$$

$$L_g = \frac{\mathrm{Im}(Z_{11})}{\omega} - L_s + C_{pg}(R_s + R_{dy} + R_g)^2 \tag{6c}$$

The value of ($R_s + R_g$) is determined by repeating the forward-biased measurement for several dc gate current levels (I_g) and plotting the

TABLE I

THE VALUES OF MEASURED S-PARAMETERS (MAGNITUDE AND PHASE) FOR THE FET BIASED TO $V_d = 1.5$ V, $V_g = 0.4$ V, $I_d = 11.1$ mA, AND THE EXTRACTED VALUES OF THE CIRCUIT ELEMENTS (UNITS ARE: FREQUENCY (GHz), PHASE (DEGREES), CAPACITANCE (fF), RESISTANCE (ohms), INDUCTANCE (pH), TRANSCONDUCTANCE (mS), AND TIME DELAY (ps)

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
5.64	0.9964	-16.81	2.4665	163.36	0.0274	75.82	0.7125	-15.03
10.43	0.9735	-30.77	2.3792	149.71	0.0499	60.37	0.7078	-27.81

Freq	C_{pg}	C_{pd}	L_g	L_d	L_s	R_d	R_s
1.64	39.09	51.42	51.67	62.80	6.58	11.99	9.14
2.44	39.07	50.58	54.18	64.99	5.44	11.93	9.19
3.24	38.22	50.14	55.73	64.05	5.75	12.00	9.15
4.04	39.89	53.30	56.56	68.09	6.63	12.00	9.11
4.84	37.94	52.30	57.47	67.00	4.01	12.04	9.15
5.64	39.40	51.94	56.43	67.13	5.03	12.04	9.18
6.44	37.95	52.36	58.65	67.28	3.76	12.04	9.20
7.24	38.24	53.58	59.38	65.57	4.64	12.15	9.21
8.04	37.54	52.67	61.41	67.20	4.61	12.23	9.22
8.84	39.21	52.34	59.19	67.94	4.46	12.23	9.20
9.63	39.31	52.40	59.00	68.63	4.17	12.18	9.23
10.43	38.69	53.28	64.15	67.04	4.34	12.14	9.28
11.23	38.22	52.35	62.78	68.94	4.12	12.32	9.25
12.03	38.02	52.63	61.30	70.52	3.60	12.20	9.31
12.83	38.82	52.25	60.74	72.47	3.59	12.38	9.33
13.63	38.13	51.86	64.85	73.28	3.41	12.37	9.34
14.43	38.91	52.53	62.52	73.33	3.49	12.49	9.32
15.23	36.95	53.13	68.34	71.84	3.51	12.34	9.40
16.03	41.05	54.04	62.18	72.15	3.09	12.47	9.37
16.83	38.43	52.58	68.20	74.13	3.92	12.50	9.50
17.63	39.57	53.44	64.79	77.56	3.89	12.26	9.38
18.42	36.93	54.10	68.28	74.32	4.61	12.49	9.38

Freq	R_g	C_{gs}	C_{gd}	R_i	G_m	τ	r_{ds}
1.64	9.10	29.22	8.99	030.49	43.93	-0.20	198.01
2.44	9.18	30.68	8.38	-44.47	43.96	01.97	199.08
3.24	9.16	31.75	8.98	-78.29	43.84	03.02	199.82
4.04	9.16	30.74	8.45	-30.10	43.38	01.07	203.02
4.84	9.22	30.34	8.17	008.65	43.54	00.16	199.89
5.64	9.19	28.23	8.56	-32.13	43.58	01.40	200.89
6.44	9.30	30.01	8.65	-24.31	43.47	01.18	202.29
7.24	9.27	29.62	8.53	-17.06	43.27	00.94	203.08
8.04	9.21	30.78	8.26	004.08	43.10	00.19	205.51
8.84	9.28	29.01	8.41	001.70	43.05	00.30	203.99
9.63	9.30	28.81	8.50	-04.31	42.95	00.44	206.09
10.43	9.60	28.60	8.59	002.60	42.62	00.26	208.45
11.23	9.39	28.50	8.46	011.46	42.58	-0.01	208.46
12.03	9.61	28.45	8.62	002.91	42.42	00.27	211.34
12.83	9.29	27.71	8.79	-19.77	42.35	00.94	214.13
13.63	9.73	28.01	8.65	000.87	41.77	00.30	214.34
14.43	9.51	27.29	8.66	010.95	41.83	00.04	217.21
15.23	9.72	28.59	8.63	-00.68	41.57	00.35	216.71
16.03	9.23	25.20	8.61	003.91	41.66	00.33	213.76
16.83	10.05	26.44	8.66	-07.27	40.76	00.52	217.79
17.63	9.47	25.52	8.68	004.00	41.12	00.31	211.84
18.42	9.96	28.10	8.52	-05.42	41.04	00.49	207.67

real part of (Z_{11}) versus the inverse of gate current $(1/I_g)$ [1]. This is a linear plot and extrapolation to $(1/I_g = 0)$ gives $(R_s + R_g)$. The measurement frequency should be sufficiently low, so that the effect of junction capacitance could be ignored.

A few comments about the frequency range of operation are in order now. The technique has been implemented only up to a frequency of about 22 GHz, because the validity of the underlying assumptions behind this technique become questionable as the frequency increases. For instance, in writing (1c), the contributions of series inductors and resistors have been neglected. This assumption could cause inaccuracies greater than 10 per cent as the frequency is increased to 30 GHz.

Equations (1), (5), and (6) were used to calculate the parasitic elements of several $0.1 \times 50\mu$m pseudomorphic MODFET's. The FET lay-outs were embedded in coplanar environment, which made them suitable for microwave on-wafer probing. The input and output pad structures consisted of coplanar lines which were 260 μm each. These line lengths guaranteed that the calibration reference planes were not within the FET gate structure. A photograph of the FET is shown in Fig. 4. The measurements were made using a 8510 HP vector network analyzer and a Cascade Microtech wafer probe station. The wafer probes were calibrated using the Line-Reflect-Match (LRM) calibration technique, and standards provided by Cascade Microtech. Current levels ranging from 8 to 18 mA were used to determine the sum $R_s + R_g$. The resistance and inductance values were determined from the measurement at 10 mA gate current. As mentioned before, the imaginary part of measured Z_{12} was negative, indicating capacitive behavior. The above equations were used to calculate the parasitic inductances. Fig. 5 shows the frequency variation of L_s, L_d and L_g for one of the devices. The variation of parasitic capacitive components with frequency is tabulated in Table I. In both cases, the values of circuit elements only vary slightly with frequency. Similar behavior has been observed for many other devices tested.

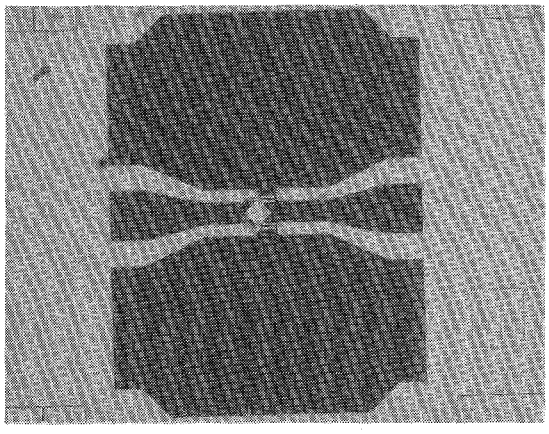

Fig. 4. A photograph of the FET structure in the coplanar waveguide environment.

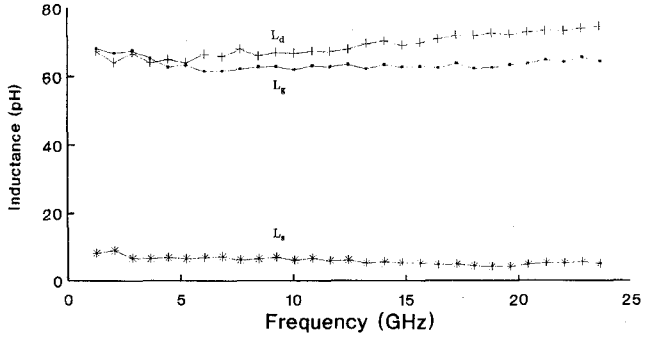

Fig. 5. Variation of the parasitic inductances with frequency.

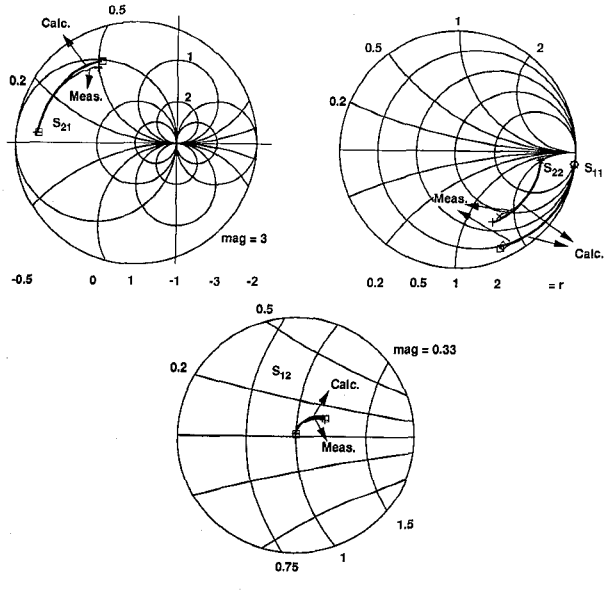

Fig. 6. Comparison of the measured and calculated S-parameters in the frequency range from 1.6 to 22.4 GHz. The calculations are based on the equivalent circuit element values extracted at 10.43 GHz.

The above technique and the equations given in [2] were used to calculate the small-signal equivalent circuit parameters of a pseudomorphic MODFET. The values of measured S-parameters under "active" ("hot") bias condition, and the variation of circuit elements with frequency are shown in Table I. Except for R_i and τ, there is little variation with frequency. Extraction of R_i is difficult since it appears in series with the capacitor C_{gs}. The reactance of C_{gs}, at the frequencies of interest, could be two orders of magnitude larger than the resistance R_i. The value of τ is also affected by the variations in R_i. In order to further investigate the influence of R_i on τ, the value of R_i was set to zero $R_i = 0.0$. The values of τ thus obtained ranged from 0.30–0.43 picoseconds for all the frequencies of Table I, except the first four which varied between 0.12 to 0.70 picoseconds. The polar plots of Fig. 6 show the measured S-parameters and those calculated based on the circuit element values of Table I at 10.43 GHz. Good agreement between the measured and calculated S-parameters is observed over the whole frequency range especially at lower frequencies.

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Microstrip Quarter-Wave High Voltage DC Block

Thomas E. Koscica

***Abstract*— A microstrip high voltage dc block is presented. Silicon rubber is used to insulate a quarter-wave coupler and the resulting effective dielectric constant and impedance are discussed. DC isolation up to 4500 V is achieved.**

I. Introduction

The need for dc blocks that can handle over several hundred volts can be grouped into two areas: First, the biasing of high voltage devices such as vacuum tubes, IMPATT devices, and electrooptic phase shifters. Second, the protection enhancement of bias tees and microwave equipment incorporating them.

Standard coupled line bias gaps, [1]–[4], have well developed microwave models with good performance for voltage supplies less than 200 V, depending on humidity. Above this bias level, attention must be given to voltage breakdown of either air or the dielectric of a lumped element capacitor where used.

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